



Digital Design with Verilog® HDL: (Formerly titled "Hardware Modeling with Verilog HDL") (Design Automation Series)

Elizer Sternheim

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Verilog HDL is the standard hardware description language for the design of digital systems and VLSI devices. This volume shows designers how to describe pieces of hardware functionally in Verilog using a top-down design approach, which is illustrated with a number of large design examples. The work is organized to present material in a progressive manner, beginning with an introduction to Verilog HDL and ending with a complete example of the modelling and testing of a large subsystem.

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